67. (New) The memory circuit of Claim 66, wherein the control logic is adapted to receive an external mode select signal for selecting the burst mode and for determining the selected mode control signal.

68. (New) The memory circuit of Claim 66, wherein the control logic includes mode circuitry for providing the selected mode control signal, the mode circuitry coupled for receiving an enable signal for determining the selected mode control signal.

69. (New) The memory circuit of Claim 68, wherein the enable signal is a write enable signal.

70. (New) The memory circuit of Claim 68, wherein the enable signal is an output enable signal.

71. (New) The memory circuit of Claim 66, wherein the selection and temporary storage circuitry is coupled to a counter, and wherein the counter is used for incrementing the first external address when in the burst mode.

72. (New) The memory circuit of Claim 66, wherein the pipelined mode and the burst mode are extended data out modes.

REMARKS

The Applicant has carefully reviewed and considered the Office Action mailed on February 1, 2001, and the references cited therewith. Claims 32 and 59 have been amended to correct a typographical error and to clarify the elements of the claim. No claims have been canceled, and claims 66-72 have been added; as a result, claims 22-32, 59-61, and 63-70 are now pending in this application.

Objection to Specification

In § 4 of the Office Action, the Office has objected to the disclosure with regard to mis-designated drawing element "MUX 123". The Applicant has amended the paragraph to remove this reference, and substitute "buffer 122" (called out in Figs. 9 and 10) therefor. No new matter has been added.

Claim Objections

In § 3 of the Office Action, claims 22, 59, 60, and 61 were objected to under 37 CFR 1.75(b) as not substantially differing from each other. The Applicant respectfully submits that claims 22, 59, and 60 are clearly different from each other. In particular, claim 22 recites a memory circuit which includes "control logic for providing a selected mode control signal". As amended, claim 59 recites a memory circuit "wherein the memory circuit is an asynchronous dynamic random access memory circuit". Claim 60 recites a memory circuit including "control logic for providing an external mode control signal". None of these elements are the same as either of the others; each has a clearly defined difference according to the recited elements.

For example, the mode control signal of claim 22 can be selected to be internal or+ external to the memory circuitry. Further, the mode control signal of claim 59 exists within an asynchronous DRAM memory circuit, as opposed to some other type of memory circuit. Finally, the mode control signal of claim 60 is external to the memory circuit, and not internal. Clearly, controlling the mode of operation by confining selection to an external signal is different than allowing other types of signals to be selected (See Applicant's specification at page 25, lines 22-24). Similarly, confining memory operations to a an asynchronous DRAM circuit is different than allowing other types of memory circuits to be used. Thus, withdrawal of this objection is respectfully requested.

§102 Rejection of the Claims

Claims 22-32, 59-61, and 63-65 were rejected under 35 U.S.C. § 102(e) as being anticipated by Manning (U.S. Patent No. 5,610,864). The MPEP requires that "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." *See* M.P.E.P. § 2131. Thus, the Applicant asserts that the Office has failed to show that Manning discusses the

identical invention claimed in the instant application, and respectfully traverses the rejection by the Office.

The Office has failed to produce a *prima facie* case of anticipation. For example, the Applicant cannot find, and the Office has failed to show, where Manning discusses the ability to switch between burst and pipelined *modes* of operation. The Office asserts that Manning discusses a pipelined mode of operation, when the actual text of Manning refers to a "pipelined architecture" as being applicable to Manning's invention (*See* Manning at column 5, lines 43-50). Does Manning refer to individually addressing and accessing memory data in a pipelined fashion, as defined by the Applicant, or merely driving data outputs in a pipelined fashion while operating in a burst mode? According to Manning, a pipelined architecture is "where memory accesses are performed sequentially, but each access requires more than one cycle to complete." This definition doesn't appear to markedly differentiate pipelined memory access from burst operations. Thus, Manning merely discloses the possibility that a pipelined *architecture* (as opposed to a mode of operation) might be "applicable to the current invention" (without disclosing how such an application might occur). Moreover, while Manning does specifically discuss the option of "switching between burst EDO and standard EDO modes of operation" (See Manning at col. 6, lines 14-16), Manning never extends this idea to switching between a pipelined *mode of operation*, and a burst mode of operation. Thus, the assertion by the Office that "Manning discloses switching between fast page pipeline and burst" is simply not supported using any of the teachings of Manning.

As the Applicant has previously explained, the EDO mode is a mode that extends the amount of time for which data is valid at the outputs of a DRAM (*See* the Applicant's specification at page 3, lines 19-21). The fast page mode is a mode that uses a row address strobe to latch a row address portion of a DRAM address (*See* the Applicant's specification at page 2, lines 12-13), while the pipelined mode is a mode that divides address information into operational times such that the address information can be provided from an external source as a stream of data (*See* the Applicant's specification at page 8, lines 1-13). The Applicant also specifically teaches *switching* between pipelined and burst modes of operation (*See* the Applicant's specification at page 26, line 24 - page 27, line 1).

The Applicant cannot find where Manning discusses that these mode are interchangeable,

or combinable, such that the term "fast page pipeline" asserted by the Office can be defined. The Applicant still fails to understand the meaning of this phrase, and looks to the Office for a more detailed explanation. Thus, the Applicant cannot find, and the Office has failed to show, a single instance where Manning discusses switching memory access activity between burst and pipelined *modes of operation*, as claimed by the Applicant in independent claims 22, 59, 60, 61, 63, and 65, and the claims which depend from them.

In short, what is discussed by Manning is not identical to the subject matter of the present invention as required by the M.P.E.P., and therefore, the rejection is improper. Reconsideration and allowance of claims 22-32, 59-61, and 63-65 is therefore respectfully requested.

New Claims

Claims 66-72 have been added. It is noted that each of claims 66-72 incorporate all of the elements of claim 22. Thus, consideration and entry of claims 66-72 is respectfully requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6913 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 1 day of May, 2001.

Tina Pugh
Name

Signature